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Comprehensive Investigation of the Side-gate Effect on the RF Small-signal Equivalent Elements of AlGaN/GaN High-Electron-Mobility Transistor on a Silicon Substrate

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Abstract—The side-gate effect on the radio frequency (RF) small-signal equivalent elements of an AlGaN/GaN HEMT on a high-resistivity silicon substrate was comprehensively studied. The side-gate bias was found to have a significant impact on the direct-current (DC) and small-signal performance of the device through the buffer layer. Gate and drain bias dependent small-signal equivalent circuit parameters were extracted at different side-gate biases, and the physical mechanism was investigated and analyzed. These findings suggest that the side-gate effects should be taken into account when monolithic microwave integrated circuits are designed based on GaN-on-Si HEMTs.

Index Terms— Gallium nitride (GaN), high electron mobility transistor (HEMT), side-gate effect, small signal equivalent-circuit

INTRODUCTION

Great progress has been made for Gallium-nitride GaN-based high electron mobility transistor (HEMT), a promising candidate for radio-frequency (RF) and microwave applications, including high power amplifiers (HPA), low noise amplifies (LNA) and monolithic microwave integrated circuits (MMICs) [1]-[6]. Although GaN-on-SiC RF devices have already achieved great success due to their advantages of high epitaxial material quality and high heat dissipation capability, GaN-on-Si RF devices are also very attractive because of their potential of being low-cost products. Owing to GaN’s wide band-gap (~3.4 eV), GaN HEMTs usually have a high breakdown voltage, which allows a high drain bias (V_{DS}), for example, 29-59 V, to be used to achieve high output power density [7]. However, in an MMIC, the performance of the GaN device

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may be influenced by its adjacent devices biased at high V_{DS}, which amounts to what is called the side-gate effect. Consequently, the side-gate effect could make the circuit design more complicated since the side-gate bias (V_{SG}) will affect the performance of the whole circuit, whose optimal performance is weakened [8] - [11]. Therefore, it is necessary to investigate the side-gate effect on the performances of the GaN HEMTs.

Some research groups have already studied the side-gate effect on gallium arsenide (GaAs) related applications. In GaAs MESFETs and HEMTs, the kink caused by the V_{SG} has been observed in direct-current (DC) I-V curve, which degrades the device performance [12] [13]. The side-gate effect was also used to modulate the 2-dimensional electron gas (2DEG) so as to study the 2DEG transport property by applying positive and negative biases to the device side gate [14]. For GaN-related applications, some research groups have investigated the side-gate influence on the GaN filter and GaN MESFET [15] [16]. In a GaN HEMT, the influence of DC and RF performance by the side-gate effect has been reported in [17]. Buffer depletion caused by the negative V_{SG} is attributed to performance degradation. In this paper, we have comprehensively analyzed the side gate influence on the RF small signal equivalent circuit components for a GaN HEMT on a high-resistivity silicon substrate.

Device Fabrication and Measurement

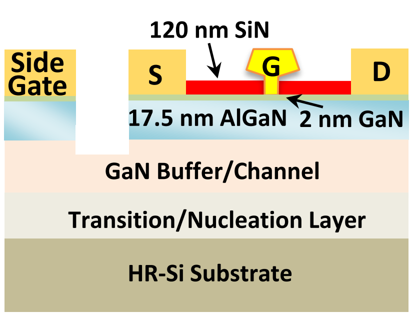


Fig. 1: Schematic diagram of the AlGaN/GaN HEMT with side gate on a high resistivity silicon substrate

Figure 1 shows the structure of the AlGaN/GaN HEMT, which was grown on a high-resistivity silicon substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial layers of the HEMT consist of a 2 nm GaN cap layer, a 17.5 nm $Al_{0.26}Ga_{0.74}N$ barrier layer, a 1.5 μm undoped GaN buffer, and a transition layer. The AlGaN/GaN HEMT fabrication was started with mesa isolation by inductively coupled plasma etching using Cl_2/BCl_3 gases with a depth of around 120 nm. Ti/Al/Ni/Au (20/140/40/50 nm) metal layers were deposited followed by rapid thermal annealing at 875 ^{o}C for 30 sec in N_2 ambient to form the source and drain Ohmic contacts. A T-shape gate with a 300 nm foot length was formed by electron beam lithography patterning, followed by Ni/Au (50/300nm) evaporation and lift-off process. Finally, a 120 nm SiN was deposited by a plasma-enhanced chemical vapor deposition (PECVD) system for surface passivation. An electrode with an Ohmic contact was fabricated 30 μm away from the source contact to work as the side gate.

In this study, three different V_{SG} values were separately applied to the side-gate to investigate their influences on the RF small signal characteristics for the GaN-on-Si HEMT. For each V_{SG} value, the DC and RF characteristics were measured and the small signal equivalent circuit elements were extracted. DC measurements were carried out with a Keithley 4200 Semiconductor Characterization System and the RF measurements were performed using an HP4142 parametric analyzer and a HP8510 network analyzer with Cascade probes.

Results and Discussion

DC and Microwave Measurement Results

Table I: Comparison of DC characteristics at different V_{SG} values

V_{SG} (V)	I_{DMAX} (mA/mm)	R_{ON} (Ω·mm)	g_{max} (mS/mm)	V_T (V)	I_{SG} (A)
100	720	4.9	224	-2.53	1.2×10^{-6}
0	693	5.2	226	-2.48	0
-100	578	5.9	214	-2.04	-4.4×10^{-6}

DC parameters including maximum drain current density (I_{DMAX}) (at V_{GS} = 1 V), on-resistance (R_{ON}), maximum transconductance (g_{max}), and threshold voltage (V_T) were listed in Table I. The V_{SG} dependent output and transfer characteristics are very similar to those in reference [17]. I_{DMAX}, g_{mmax} and V_T are measured at different V_{SG} while at the same drain bias (V_{DS}) of 10 V. I_{DMAX} was found to decrease when V_{SG} = -100 V and increase when V_{SG}=100 V compared with the I_{DMAX} value at V_{SG}=0 V. The R_{ON} is reduced when biased at V_{SG}=100 V and increased at V_{SG}=-100 V. The V_T is slightly negatively shifted when V_{SG}=100 V and positively shifted when the device is biased at V_{SG} = -100 V. It is believed that the electrical field effect induced by the side-gate bias is attributed to those changes [18]. The positive V_{SG} will serve as the positive back-gate to attract electrons in the 2DEG channel and thus increase the 2DEG density which results in an increased I_{DMAX}, reduced R_{ON}, and negatively shifted V_T. For a similar reason, the negative V_{SG} will deplete the 2DEG in the channel and thus decrease I_{DMAX}, increases R_{ON}, and positively shift V_T. There is a slight decrease of the g_{mmax} when V_{SG}=100 V, however when V_{SG}=-100 V g_{mmax} is significantly decreased due to the buffer depletion and deep level donor trap ionization which enhances the scattering of the 2DEG carriers. Because of the enhanced scattering, the electron mobility in the channel is reduced so that the g_{mmax} at V_{SG}=-100 V is reduced.

Figure 2(a) shows the measured cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) of the GaN HEMT on Si as a function of V_{GS} at three different V_{SG} and fixed V_{DS} = 10 V. It can be noticed that at V_{SG}=100 V and V_{SG}=-100 V both the f_{max} and f_t are reduced compared to that at V_{SG}=0 V. The f_t value when the side gate is biased at V_{SG}=0 V is 23 GHz while it is decreased by 4% and 17% when the side gate is biased at V_{SG}=100 V and V_{SG}=-100 V, respectively. The decrease of the f_{max} and f_t for V_{SG}=-100 V is caused by the decrease of the electron mobility due to the electrical field effect as above mentioned [16]-[18]. As to the slight decrease of the f_{max} and f_t at V_{SG}=100 V when compared with that at V_{SG}=-100 V it is attributed to the electron shielding effect which reduces the scattering.

Figure 2(b) shows the measured f_t and f_{max} as a function of V_{DS} for three V_{SG}. Over the whole V_{DS} range, the change of the f_t and f_{max} values with V_{SG} stays the same. There is a slight decrease of the f_t and f_{max} when V_{DS} increases. It is assumed that the hot electrons should be attributed to this decrease. When V_{DS} increases, the hot electrons are generated and then captured by the traps and defects which reduce the electron mobility and velocity in the 2DEG channel by producing enhanced scattering. Therefore, the electron mobility and velocity in the 2DEG channel is reduced, resulting in a reduced f_t and f_{max}.

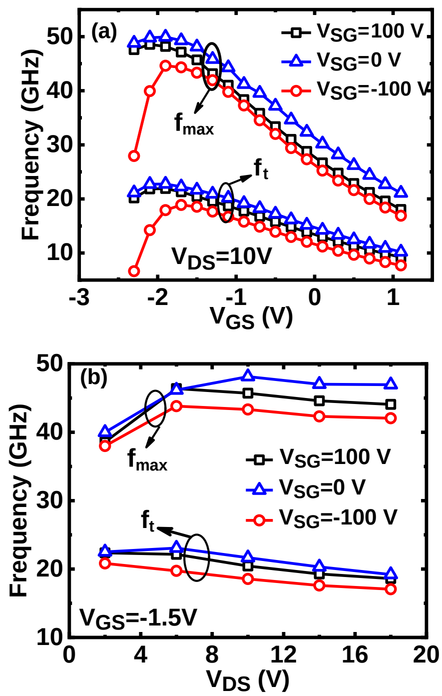


Fig. 2: Measured f_t and f_{max} values versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

B. Extracted Small Signal Equivalent Circuit Parameters

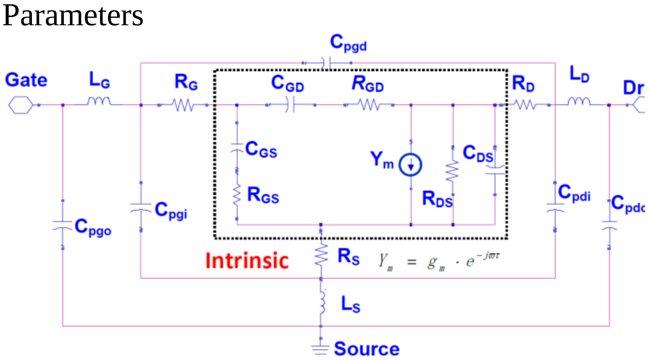


Fig. 3: Schematic of a small-signal equivalent circuit [15].

A small-signal equivalent circuit of the GaN HEMT on high-resistivity silicon is shown in Fig. 3. The detailed definitions and the extraction procedures of those small-signal equivalent circuit parameters (ECPs) are the same as in reference [19].

Table II: Comparison of access resistance at three side gate voltages

	V_{SG}=-100 V (Ω·mm)	V_{SG}=0 V (Ω·mm)	V_{SG}=100 V (Ω·mm)
R_D	1.8	1.5	1.5
R_S	0.9	0.8	0.8

Table II lists the extracted drain (R_D) and source (R_S) access resistance at different V_{SG}. There is almost no R_S and R_D difference between the V_{SG}=0 V and V_{SG}=100 V. At V_{SG}=-100 V, both the R_S and R_D are increased due to the reduced 2DEG density and mobility resulted from the electrical field effect as aforementioned.

Figure 4 shows the extracted g_m as a function of V_{GS} and V_{DS} at three different V_{SG}. The trend of g_m varying with the change of the V_{GS} and V_{DS} is consistent with the measured f_t, which stays the same for the three V_{SG}. The change of the g_m versus V_{GS} and V_{DS} reflects the electrons mobility and velocity change in the 2DEG channel. The decrease of the g_m when V_{SG}=-100 V is mainly due to the decrease in the electron mobility and effective velocity caused by the enhanced Coulomb scattering. The decrease of the g_m with the increase of the V_{DS} is attributed to the hot electron effect as aforementioned.

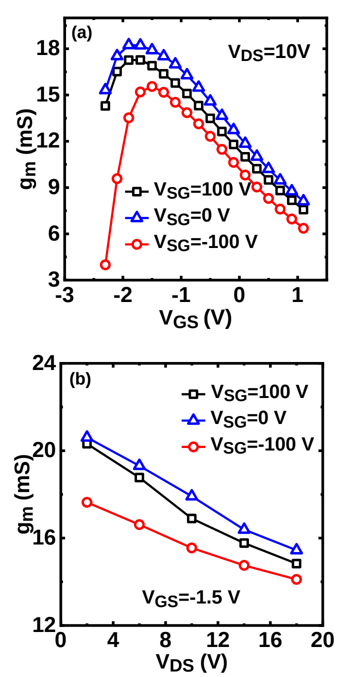
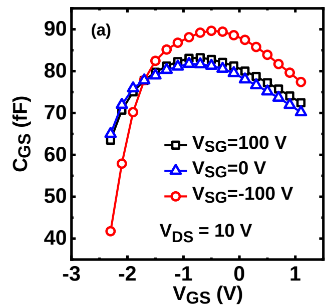


Fig. 4: Extracted intrinsic g_m versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}

Figure 5 shows the V_{GS} and V_{DS} dependent gate to source capacitance (C_{GS}) at three different V_{SG}. As shown in Fig. 5(a), C_{GS} first increases with the increase of the V_{GS} and then slightly decreases with the increase of the V_{GS}. The same phenomenon has been observed for GaN HEMT by other groups [20]-[22]. The decrease of C_{GS} with the increase of V_{GS} is believed to be caused by the nonlinear source resistance. When V_{GS} is high, some of the electrons in the 2DEG channel will spill into the barrier layer to form parallel MESFET conduction. The spilled electrons will be captured by the traps and defects in the barrier and AlGaN/GaN interface. As a result, the electrons in the 2DEG channel will be depleted which leads to the reduction of the C_{GS} at high V_{GS} especially when the frequency is above GHz. This phenomenon is also observed in GaAs HEMTs [23]. When $V_{GS} < -2$ V, C_{GS} at V_{SG}=-100 V decreases much faster with the V_{GS} decrease compared with that at V_{SG} = 0 V and 100 V. The channel depletion induced more positive V_T at V_{SG}=-100 V is attributed to this more rapid decrease. When V_{SG} = -100 V, the negative V_{SG} will deplete the channel and result in a reduced 2DEG density, and thus at the same negative V_{SG} (< -2 V) the device is operating closer to the V_T region so that the channel is more depleted compared with that at V_{SG}=0 V and 100 V, leading to a lower C_{GS}.

When V_{GS} is larger than -1.7 V and the device is working at on-state, the C_{GS} value at V_{SG} = -100 V is obviously larger than the C_{GS} value at V_{SG}=100 V and 0 V, while the similar C_{GS} value is exhibited between V_{SG}=100 V and 0 V for the same V_{GS} and V_{DS}. When V_{SG} = -100 V, the depletion depth in the channel layer at the source side of the gate was reduced and the nominal gate to 2DEG distance is reduced, resulting in an increased C_{GS}. This can be explained when V_{SG} = -100 V, the substrate was applied with a negative bias forming a back-gate, the electrons in the channel layer were pushed forward to the gate and entered into the channel depletion layer. When the electrons enter into the source to gate channel depletion region, the depletion height was reduced and the 2DEG locates closer to the gate electrode, leading to the increase of the C_{GS} at V_{SG} = -100 V compared with the C_{GS} value at two other bias conditions. As to the similar C_{GS} value observed between the V_{SG} = 0 V and 100 V, the buffer electrons shielding effect should be attributed to this phenomenon. When V_{SG}=100 V, part of the electrons in the channel will enter the buffer layer, serving as the shielding electron layer and preventing more electrons from entering the buffer layer which indicates as the shielding effect similar to the MESFET conduction formation in the $Al_{0.26}Ga_{0.74}N$ layer when the gate was applied with positive bias. Therefore, the depletion between the gate and source is less influenced by the positive V_{SG}. Consequently, the extracted C_{gs} values are less influenced by the positive V_{SG} while it is significantly influenced by the negative V_{SG}.

Figure 6 (b) shows the extracted C_{GS} versus V_{DS} at a fixed V_{GS} = -1.5 V for a frequency range of 1-20 GHz. The C_{GS} first increases with the increase of the V_{DS} and after reaching its peak value, it almost stays constant over the whole V_{DS} range. This trend remains the same for three V_{SG} conditions. The increase of the C_{GS} along with the increase of the low V_{DS} is due to the fact that the device operates at the liner region before it reaches the saturation region. When it works in the saturation region at a higher V_{DS}, the gate-to-source depletion almost remains the same and will not vary obviously with the increase of the V_{DS}. At the saturation region, the C_{GS} values at V_{SG}=-100 V is larger than C_{GS} at V_{SG} = 0 V and V_{SG} = 100 V which shows the same trend as in Figure 6 (a).



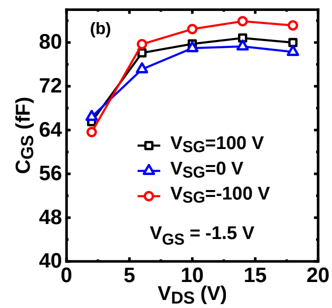


Fig. 5: Extracted C_{GS} versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

The extracted gate-drain capacitance (C_{GD}) versus V_{GS} for the GaN HEMT with different V_{SG} conditions is shown in Fig. 6(a). At low V_{GS} (< -2 V), the C_{GD} decreases with the increase of the V_{GS}, after reaching its minimal value C_{GD} increases with the increase of the V_{GS} for all V_{SG} conditions. When the V_{GS} is less than -2 V, C_{GD} at V_{SG} = -100 V increases faster with the V_{GS} decrease than those at V_{SG} = 0 V and V_{SG} = 100 V, which is shown in Fig. 6(a) as the crossing of the three curves at a low V_{GS}. It is related to the fact that at V_{SG} = -100 V the device is biased closer to the pinch-off condition when V_{GS} is smaller than -2 V, similar to the case of C_{GS} versus V_{GS} as shown in Fig. 6(a). Fig. 6(b) shows the C_{GD} versus V_{DS} at different V_{SG} values. C_{GD} decreases with the increase of the whole V_{DS}, and this trend remains the same for three V_{SG} conditions. Both in Fig. 6(a) and Fig. 6(b), the C_{GD} value at the V_{SG} = 0 V is only slightly larger than that at V_{SG} = 100 V, while it is much larger than that at V_{SG} = -100 V for the same V_{DS} and V_{GS} (> -2 V).

When a HEMT is biased at its saturation region, C_{GD} can be roughly expressed as the following equation [20]:

$$C_{GD} = \frac{\varepsilon W_G(d + \Delta d)}{L_{GD,eff}}$$

where d is the distance from gate to the barrier/channel hetero-junction interface, and Δd is the effective distance from the hetero-junction interface to the 2DEG cloud, and $L_{GD,eff}$ is the effective distance of the gate-drain spacing. The symbol ε denotes the dielectric constant of the $Al_{0.26}Ga_{0.74}N$ and W_G is the gate width. For a relatively high V_{GS}, when V_{GS} increases, the effective depletion length L_{gdeff} at the drain side of the gate is reduced. In addition, Δd becomes less sensitive to the V_{GS} because at a high V_{GS}, Δd is closer to 0 nm which becomes neglected compared with d, thus C_{GD} increases when V_{GS} increases at a high V_{GS}. On the contrary, when V_{DS} increases the $L_{GD,eff}$ increases and thus C_{GD} decreases.

In addition, when V_{SG} = -100 V, the negative back gate voltage induced by the large negative V_{SG} reduces the 2DEG density and thus increases the effective depletion length from gate to drain electrodes ($L_{GD,eff}$). So the C_{GD} values at V_{SG} = -100 V are much smaller than those at V_{SG} = 0 V. While at V_{SG} = 100 V, the induced positive back gate voltage weakens the 2DEG pinch-off at the gate edge close to the drain, so that the pinch-off point in the channel moves to the drain, resulting in the $L_{GD,eff}$ increase and C_{GD} decrease. While on the other side, the positive back gate voltage would also make the 2DEG cloud center move a bit towards the substrate and increase the Δd. Those two effects counteract each other so that the C_{GD} value at V_{SG}=100 V is slightly smaller than that at V_{SG}=0 V.

Figure 7 depicts the drain-to-source capacitance (C_{DS}) as a function of V_{GS} and V_{DS}. In Fig. 7(a), it was found that C_{DS} increases with the increase of V_{GS} (near pinch-off) to its peak value and then decreases when V_{GS} keeps increasing. In Fig. 7(b), the C_{GD} decreases with the increase of V_{DS}. The trend remains the same for the three V_{SG} conditions. For both figures, the values of C_{DS} for V_{SG} = -100 V are larger than the C_{DS} value for V_{SG} = 0 V, which is also larger than that value at V_{SG} = 100 V at the same V_{DS} and V_{GS} (V_{GS} > -2 V).

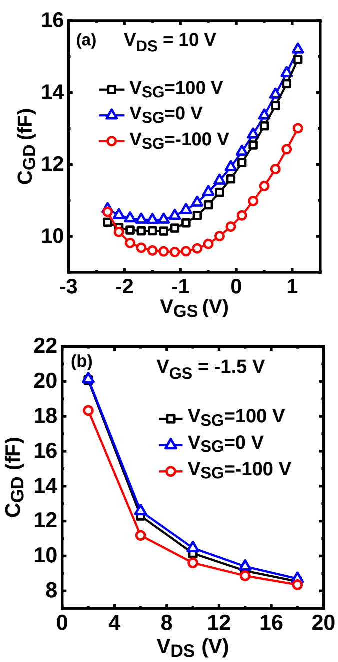


Fig. 6: Extracted C_{GD} versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

The C_{DS} values can be roughly estimated as [25]

$$C_{DS} = \frac{\varepsilon 2\pi h(V_{gs}, V_{ds})}{L}$$

Where $h(V_{GS}, V_{DS})$ represents the depletion height in the channel and L represents the channel depletion length.

At low V_{GS} < -2 V, the channel is severely depleted and thus the h is almost constant, the L value increases when the V_{GS} value was further decreased and thus reduces C_{DS}. When V_{GS} is larger than -2 V and keeps increasing, the channel depletion is reduced and L is almost equal to the gate length. In this case, the channel depletion height h is reduced which results in a decreased C_{DS}. Therefore, C_{DS} first increases with the increase of V_{GS} and then decreases with the increase of V_{GS}. As a comparison, the L increases along with the increase of V_{DS} at a fixed V_{GS}=-1.5, resulting in a decreased C_{DS} as V_{DS} is increased.

When the side gate is biased with a large negative voltage V_{SG} = -100 V, the induced negative back gate enhances the channel and buffer depletion, so that $h(V_{GS}, V_{DS})$ becomes higher and C_{DS} becomes lower. Similarly, when V_{SG} = 100 V the channel depletion height h is smaller and C_{DS} becomes lower. At low V_{DS} i. e. in the linear operation region, the C_{DS} value at V_{SG}=-100 V is lower than that at V_{SG}= 0 V, which is because that at the linear region, the 2DEG at the gate edge close to the drain is not depleted so C_{DS} is related to the 2DEG density. At V_{SG}=-100 V, the 2DEG is depleted by the negative back gate voltage so C_{DS} becomes smaller.

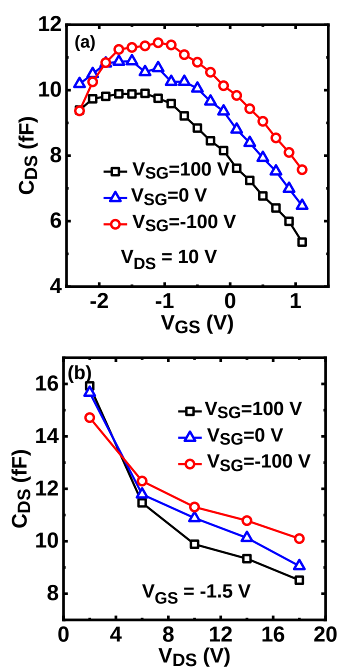


Fig. 7: Extracted C_{DS} as a function of the (a) V_{GS} and,
(b) V_{DS} at three different V_{SG}

Figure 8 shows the extracted effective electron velocity (ν_{eff}) under the gate region as a function of the V_{GS} and V_{DS} at various V_{SG}. The ν_{eff} was calculated from:

$$V_{eff} = f_{t,int} \times 2\pi L_g$$

Where $f_{t,int}$ and L_g are the extracted intrinsic cut-off frequency and gate length, respectively. The change of ν_{eff} versus V_{DS} and V_{GS} is consistent with the change of the f_t versus V_{DS} and V_{GS} which reflects the electron velocity change at different V_{SG}. It can be directly seen that the 2DEG channel velocity was reduced by the enhanced scattering at large side-gate biases, especially at large negative side-gate bias.

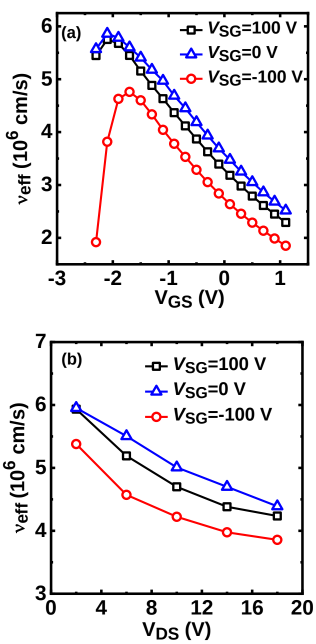


Fig. 8: Calculated ν_{eff} versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

The extracted drain to source resistance (R_{DS}) versus V_{GS} and V_{DS} are plotted in Figure 9. R_{DS} decreases with the increase of the V_{GS}, due to the increase of the 2DEG density. In Fig. 9(b), R_{DS} increases with the increase of V_{DS}, because of the enhanced gate to drain depletion when V_{DS} increases. Similar to the influence of the side gate bias on the DC access resistances R_S and R_D, R_{DS} increases obviously over the whole gate bias range and drain bias range at V_{SG}=-100 V, while it slightly decreases at V_{SG}=100 V. At low V_{GS} < -2 V and V_{SG} = -100 V, the R_{DS} drops faster when V_{GS} increases, compared with the cases at V_{SG} = 100 V and V_{SG} = 0 V. This is because at low V_{GS} and V_{SG} = -100 V the device is operating close to pinch off or subthreshold region. Thus, a little increase in the V_{GS} will lead to a significant decrease in R_{DS}. Different R_{DS} values at different V_{SG} are also attributed to the different 2DEG density and electron velocity. When V_{SG} = 100 V, on one hand, the positive V_{SG} attracts electrons and thus increases the 2DEG density in the channel; on the other hand, the electrons enter the buffer layer which forms the buffer shielding electrons to stop the electrons from keeping attracted in the 2DEG channel. Thus, the I_D is slightly increased and the R_{SH} and R_{DS} are slightly decreased. Compared to the condition at V_{SG} = -100 V, the buffer depletion was enhanced with positive charges left behind and thus the Coulomb scattering was enhanced. The mobility and velocity of the electron in the channel are reduced due to the enhanced scattering. Additionally, the electrical field effect of V_{SG} = -100 V depletes the channel with reduced 2DEG density which also increases the R_{DS}. Thus, R_{DS} value at V_{SG}=-100 V is much larger than the R_{DS} value at V_{SG}=0 V, which is slightly larger than the R_{DS} value at V_{SG}=100 V for the whole V_{GS} and V_{DS}.

Figure 10 describes the gate to source resistance (R_{GS}) and gate to drain resistances (R_{GD}) as a function of V_{DS} and V_{GS}. The accurate extractions for the two parameters are difficult and their physical source is still unclear yet, however, it is necessary to include those two parameters so as to improve the agreement between the measured and simulated S parameters [26]. The influence of the side gate bias on the values of R_{GD} and R_{GS} follows the same trend as that on R_{DS}. It is believed that similar physical mechanisms contribute to the side-gate influence.

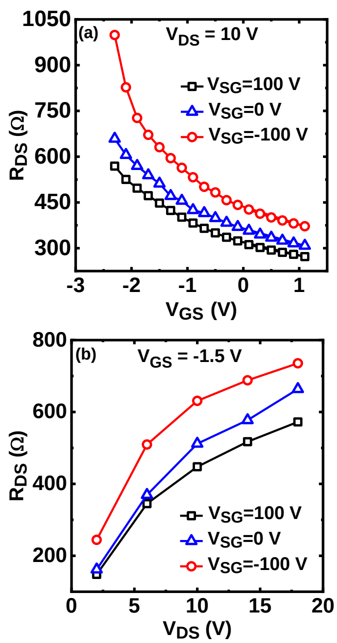
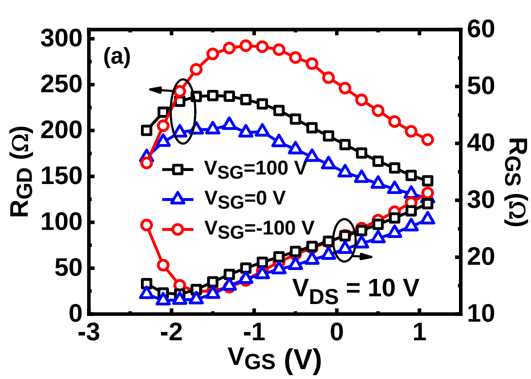


Fig. 9: Extracted R_{DS} versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

Figure 11 plots the bias-dependent time constant τ versus V_{GS} and V_{DS} at three V_{SG} conditions. The accurate extraction of τ is also challenging as the extraction of the R_{GD} and R_{GS}. In Fig. 11(a), τ first decreases with the increase of the V_{GS} and then increases with V_{GS}. In Fig. 11(b), τ increases with the increase of V_{DS} over the whole V_{DS} range. For two figures, τ at V_{SG} = -100 V is larger than τ at V_{SG} = 0 V and V_{SG} = 100 V. It is presumably believed that different buffer depletions were attributed to the increase of τ.



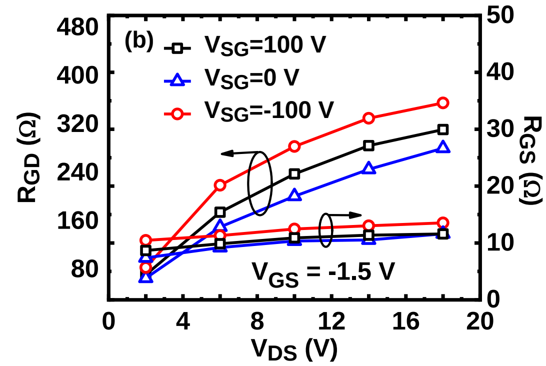


Fig. 10: Extracted R_{GD} and R_{GS} versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

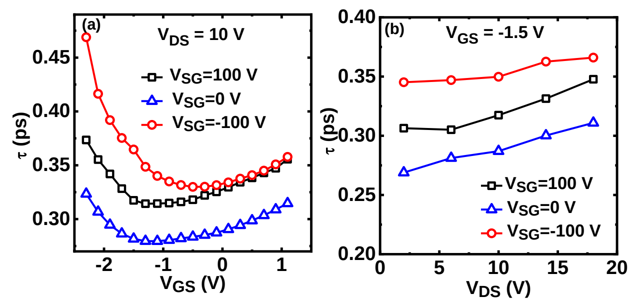


Fig. 11: Extracted intrinsic time constant τ versus (a) V_{GS} and (b) V_{DS} at three different V_{SG}.

Conclusion

In conclusion, the side gate bias was found to have an obvious influence on the RF small signal performance over a wide gate and drain bias range in an AlGaN/GaN HEMT on a silicon substrate. It changes almost all the equivalent circuit parameters. At a large negative side gate bias, e.g. V_{SG} = -100 V, the buffer depletion was induced, and hence, the channel electron depletion and Coulomb scattering were enhanced, leading to the decrease of the 2DEG density, mobility, and velocity, and hence R_{DS}, R_{GS}, R_{GD} are increased and I_{DMAX}, g_m, v_{eff}, , f_{max} and f_t are decreased. At a large positive side gate bias, e.g. V_{SG} = 100 V, the influence on the equivalent circuit parameters is much smaller due to the buffer electrons shielding effect. The electrical field distribution in the channel at different V_{DS} and V_{GS} values was also changed by V_{SG}. The combination of different factors as aforementioned arouses the difference of the small-signal parameters. The side-gate effect on the small signal ECPs need to be taken into consideration during the design of high-performance GaN MMICs.

References

[1] **K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. J. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. M. Asbeck,** and **M. Micovic**, Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency, *IEDM Tech*. Dig., pp. 19.1.1–19.1.4 (**2011**)

[2] **Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena,** and **H. Xing**, InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz, *IEEE Electron Device Letters*, **33**, no. 7, pp. 988–990, Jul. 2012.

[3] **D. Lee, X. Gao, S. Guo, D. Kopp, P. Fay,** and **T. Palacios**, 300-GHz InAlN/GaN HEMTs with InGaN back barrier, *IEEE Electron Device Lett.*, **32**(11), pp. 1525–1527, (**2011**).

[4] **Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra,** and **P, Parikh,** 30-W/mm GaN HEMTs by field plate optimization, *IEEE Electron. Device Lett.*, **25**(3**)**, pp. 117-119, (**2004**).

[5] **H. Zhou, X. B. Lou, N. J. Conrad, M. W. Si, H. Wu, S. Alghamdi, S. P. Guo, R. G. Gordon,** and **P. D. Ye,** High Performance InAlN/GaN MOSHEMTs Enabled by Atomic Layer Epitaxy MgCaO as Gate Dielectric, *IEEE Electron Device Lett.*, **37**(5), pp. 556-559, (**2016**).

[6] **Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo, V. Sahmuganathan, T. Xu,** and **C. H**. Lee, High microwavenoise performance of AlGaN/GAN MISHEMTs on silicon with Al2O3 gate insulator grown by ALD, *IEEE Electron Device Lett.*, **31**(2), pp. 96–98, (**2010**).

[7] **U. K. Mishra, P. Yi, S. Newman, R. Chu, C. Zhen,** and **S. P. DenBaars**, MOCVD-grown AlGaN buffer GaN HEMTs With V-gates for microwave power applications, *IEEE Electron Device Lett.*, **30**(9), pp. 910-912, (**2009**).

[8] **H. Zhou *et al.***, DC and RF Performance of AlGaN/GaN/SiC MOSHEMTs With Deep Sub-Micron T-Gates and Atomic Layer Epitaxy MgCaO as Gate Dielectric, *IEEE Electron Device Letters*, **38**(10), pp. 1409-1412, (**2017**)

[9] **D. Nirmal, L. Arivazhagan, A. S. Augustine Fletcher, J. Ajayan,** and **P. Prajoon**, Current collapse modeling in AlGaN/GaN HEMT using small signal equivalent circuit for high power application, *Superlattices and Microstructures*, **113**, pp. 810-820, (**2018**).

[10]**G. Zhu, C. Chang, Y. Xu, A. A. Al-Saman** and **F. Lin,** A Small-Signal Model Extraction and Optimization Method for AlGaN/GaN HEMT Up to 110 GHz, *2019 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Chengdu, China, pp. 111-112 (**2019**)

[11]**N. M. Shrestha, Y. Li, T. Suemitsu** and **S. Samukawa,** Electrical Characteristic of AlGaN/GaN High-Electron-Mobility Transistors With Recess Gate Structure, *IEEE Transactions on Electron Devices*, **66**(4), pp. 1694-1698, (**2019**).

[12]**Alan Harrison**, Back gating in Submicrometer GaAs MESFET's Operated at High Drain Bias, *IEEE Electron Device Lett.*, **13**(7), pp. 381-383, (**1992**).

[13] **H. I. Fujishiro, T. Saito,** and **S. Nishi,** Side gating effects in Inverted AlGaAs/GaAs HEMT , *Jap. Journal of Appl. Phys.*, **27**(9), pp. L1742-L1745,(**1988**).

[14] **K.Hirakawa, H.Sakaki** and **J. Yoshino,** Mobility Modulation of the Two-Dimensional Electron Gas Via Controlled Deformation of the Electron Wave Function in Selectively Doped AlGaAs-GaAs Heterojunctions , *Phys. Review Lett.*, **54**(12), (**1985**).

[15] **Shigekawa, Naoteru, Nishimura, Kazumi Yokoyama, Haruki,** and **K. Hohkawa,** Side-

gate effects on transfer characteristics in GaN-based transversal filters, *Appl. Phys. Lett.*, **87**(8), pp 1-3, (**2005**).

[16] **T. Egawa, H. Ishikawa, T. Jimbo** and **M. Umeno,** Side gating effect of GaN MESFETs grown on sapphire substrate, *Electronics Lett.*, **34**(6), pp. 598-600, (**1998**).

[17] **H. Zhou, G. I. Ng, Z. H. Liu,** and **S. Arulkumaran,** Side-gate effects on the direct current and radio frequency characteristics of AlGaN/GaN high-electron-mobility transistor on Si , *Appl. Phys. Lett.*, **99**(16), pp. 163505-1-163505-3, (**2011**).

[18] **N.Goto, Y. Ohno,** and **H. Yano,** Two-Dimensional Numerical Simulation of Side-Gating Effect in GaAs MESFET's, *IEEE Trans. On Electron Devices*, **37**(8), pp. 1821-1827, (**1990**).

[19] **Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo,** and **V. Sahmuganathan,** Comprehensive Study on the Bias-Dependent Equivalent-Circuit Elements Affected by PECVD SiN Passivation in AlGaN/GaN HEMTs, *IEEE Trans. on Electron Device*, **58**(2), (**2011**).

[20] **F. van Raay, R. Quay, R. Kiefer,M. Schlechtweg,** and **G.Weimann,** Large signal modeling of AlGaN/GaN HEMTs with Psat > 4 W/mm at 30 GHz suitable for broadband power applications, *in Proc. IEEE MTT-S Int. Microw. Symp.*, **1**, pp. 451–454, (**2003**).

[21] **J. W. Lee** and **K. J. Webb,** A temperature-dependent nonlinear analytic model for AlGaN-GaN HEMTs on SiC, *IEEE Trans. Microw. Theory Tech.*, **52**(1), pp. 2–9, (**2004**).

[22] **J. Deng, W. Wang, S. Halder, W. R. Curtice, J. C. M. Hwang, V. Adivarahan,** and **M. A. Khan,** Temperature-dependent RF large-signal model of GaN-based MOSHFETs, *IEEE Trans. Microw. Theory Tech.*, **56**(12), pp. 2709–2716, (**2008**).

[23] **I. Kallfass, H. Schumacher,** and **T. J. Brazil,** A unified approach to charge-conservation capacitance modeling in HEMTs, *IEEE Microw. Wireless Comp. Lett.*, **16**(12), pp. 678-680, (**2006**).

[24] **S. S. Islam** and **A. F. M. Anwar,** Temperature dependent nonlinearities in GaN/AlGaN HEMTs, *IEEE Trans. Electron Devices*, **49**(5), pp. 710–717, (**2002**).

[25] **J. Mateos, T. González, D. Pardo, P. Tadyszak, F. Danneville,** and **A. Cappy,** Noise analysis of 0.1 μm gate MESFETs and HEMTs, *Solid State Electron*, **42**(1), pp. 79–85, (**1998**).

[26] **M. M. Ahmed,** An improved method to estimate intrinsic small signal parameters of a GaAs MESFET from measured DC characteristics, *IEEE Trans. Electron Devices*, **50**(11), pp. 2196–2201, (**2003**).

دراسة تفصيلية لتأثير حث البوابات الجانبية على العناصر المكافئة لنموذج الإشارات الصغيرة في ترانزستورات الالكترونيات عالية الحركية المصنوعة من نيتريد الألومنيوم ونيتريد الجاليوم على ركيزة من السيليكون

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مستخلص. تم دراسة تأثير الحث الكهربي لبوابات (Gate) الترانزستورات المجاورة (الجانبية) على العناصر المكافئة لنموذج الإشارات الصغيرة (Small–signal model) لترانزستور HEMT المصنوع من مادة (AlGaN/GaN) وتأثير ذلك على الركائز العازلة من السيليكون بشكل شامل. وجد أن تأثير البوابات المجاورة يؤثر بشكل كبير ومباشر على الأداء في التيار المستمر (DC) والإشارات الصغيرة للجهاز من خلال الطبقة الناقلة (Buffer Layer). كما تم استخراج معاملات الدائرة المعادلة للإشارات الصغيرة المعتمدة على جهد المرتبط بالبوابة والمصرف أثناء توصيل بوابات جانبية مختلفة. في هذه الورقة كذلك، تم دراسة الأداء من النواحي الفيزيائية وتحليلها. تشير هذه النتائج إلى أنه يجب مراعاة تأثير الحث الكهربي لبوابات الأجهزة المجاورة عند تصميم أجهزة الدوائر الميكروويفية المتكاملة والمجمعة والمصنوعة من عنصر نيترات الجاليوم (GaN) بشكل عام والمبنية على أي ركيزة السيليكية.

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